

<b>Notice of References Cited</b>	Application/Control No. 10/708,056		Applicant(s)/Patent Under Reexamination CLARKE ET AL.	
	Examiner Vuthe Siek		Art Unit 2825	Page 1 of 1

#### U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,904,578	06-2005	Jain et al.	716/5
*	B	US-7,047,139	05-2006	Shtrichman, Ofer	702/22
*	C	US-2004/0078674	04-2004	Raimi et al.	714/033
*	D	US-2004/0019468	01-2004	De Moura et al.	703/2
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

#### FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

#### NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Clarke et al., "HARDWARE VERIFICAITON USING ANSI-C PROGRAMS AS A REFERENCE," DAC, JAN 2003, PP. 308-311.
	V	Biere et al., "SAT AND ATPG: BOOLEAN ENGINES FOR FORMAL HARDWARE VERIFICATIOIN," IEEE, FEB 2002, PP. 782-784.
	W	Clarke et al., "BEHAVIORAL CONSISTENCY OF C ADN VERILOG PROGRAMS USING BOUNDED MODEL CHECKING," DAC,, JUNE 2003.
	X	Cabodi et al., "CAN BDDs COMPETE WITH SAT SOLVERS ON BOUNDED MODEL CHECKING", DAC, JUNE 2002, PP. 117-122.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.